<table>
<tr><td>NAME OF THE COURSE</td><td colspan="5">Computer Architecture Practicum</td></tr>
<tr><td>Code</td><td>PMIC11</td><td>Year of study</td><td colspan="3">UGU-2</td></tr>
<tr><td>Course teacher</td><td>prof.dr. sc. Andrina Granić</td><td>Credits (ECTS)</td><td colspan="3">2,0</td></tr>
<tr><td rowspan="2">Associate teachers</td><td rowspan="2">dr. sc. Jelena Nakić</td><td rowspan="2">Type of instruction (number of hours)</td><td>L</td><td>S</td><td>E</td><td>F</td></tr>
<tr><td></td><td></td><td>30</td><td></td></tr>
<tr><td>Status of the course</td><td>compulsory</td><td>Percentage of application of e-learning</td><td colspan="3">25%</td></tr>
<tr><td colspan="6">COURSE DESCRIPTION</td></tr>
<tr><td>Course objectives</td><td colspan="5">To acquire knowledge about digital circuits and systems and about their application in computer architecture. To master building and analyzing digital circuits that are used for implementation of complex logical functions in digital computer.</td></tr>
<tr><td>Course enrolment requirements and entry competences required for the course</td><td colspan="5">Course enrolment requirements: none. Entry competences: basic computer experience.</td></tr>
<tr><td>Learning outcomes expected at the level of the course (4 to 10 learning outcomes)</td><td colspan="5">Students will be able to:
1. Build and analyze logical circuits
2. Classify complex logical circuits, both combinational and sequential
3. Analyze complex logical functions
4. Project digital circuits for implementation of complex logical functions
5. Compare basic implementations of digital circuits
6. Calculate performances of digital systems</td></tr>
<tr><td>Course content broken down in detail by weekly class schedule (syllabus)</td><td colspan="5">1. Introduction to the course. Introduction to the tool for designing and simulating digital logic circuits – Logisim. Designing circuits according to logical scheme. (2 hours)
2. Implementation of a logical function. Standard forms of functions. Integrated circuits technology. Cost and delay of a circuit. Logical scheme transformation into NAND and NOR form. Cost and delay analysis in respective implementations. (2 hours)
3. Minimization of logical functions. Minimization of incompletely specified functions. Minimization of maxterms products. Conversion of function into NAND/NOR form in Logisim. (2 hours)
4. Combinational logical circuit: Priority encoder, Decoder, Multiplexer. Implementation and cascading of combinational circuits. (2 hours)
5. Arithmetic circuits: Half-adder, Full adder, Substractor, Multiplier, Shifter. Designing sub circuits.
6. Programmable modules. Programmable and semi-programmable logic array. (2 hours)
7. Sequential logical circuits. Flip-flop circuits (SR, JK, T, D). Flip-flop circuits with improved control. Double flip-flop circuits. (2 hours)
8. Standard sequential modules: Registers. Register with parallel input. Shift register. Counters. Binary counter. Counter modulo m. Reverse binary counter. Add/subtract counter. Synchronous counters (binary and decimal). Decoding the counter state. (2 hours)
9. Midterm exam.
10. Comparisons of different microprocessor architectures. Selection and analysis of selected architecture for modelling in simulator. (2 hours)
11. Designing arithmetic-logic unit. Internal registers, program counter and stack pointer. (2 hours)</td></tr>
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	12. Designing control unit and bus. Review and purpose of control signals. Data flow analysis. (2 hours) 13. Design and implementation of memory modules (RAM and ROM). (2 hours) 14. Assembling parts of microprocessor. Test and analysis of model. (2 hours) 15. Final exam.
Format of instruction	☐ lectures ☐ seminars and workshops ☒ exercises ☐ on line in entirety ☒ partial e-learning ☐ field work ☐ independent assignments ☐ multimedia ☒ laboratory ☐ work with mentor ☐ homework assignments
Student responsibilities	Attendance of classes. Active involvement in classes. Midterm exam and final exam at computer.

Screening student work *(name the proportion of ECTS credits for each activity so that the total number of ECTS credits is equal to the ECTS value of the course)*

Name	Ects	Name	Ects	Name	Ects
Class attendance	1	Research		Experimental work	
Oral exam		Report		Homework assignments	
Seminar essay		Essay			
Tests		Practical training			
Written exam	1	Project			

Grading and evaluating student work in class and at the final exam	Midterm exam and final exam (50% + 50%) Complete exam (100%) Midterm exam and final exam substitute the complete exam.

Required literature (available in the library and via other media)

Title	Number of copies in the library	Availability via other media
1. U. Peruško, Digitalna elektronika, logičko i električko projektiranje, III. prošireno izdanje, Školska knjiga - Zagreb, 1996	10	
2. S. Ribarić: Građa računala: arhitektura i organizacija računarskih sustava, Algebra, Zagreb, 2011	15	
3. J. Nakić: Lecture notes	0	online

Optional literature (at the time of submission of study programme proposal)	U. Peruško, V. Glavinić: Digitalni sustavi, Školska knjiga, 2005 A. S. Tanenbaum: Structured Computer Organization. Prentice-Hall International, Third Edition, 1990.

	J. L. Hennessy and D. Patterson: Computer Architecture, A Quantitative Approach, Morgan Kaufmann Publication, Third Edition, 2003.
Quality assurance methods that ensure the acquisition of exit competences	Communication with students, students' evaluation through anonymous surveys, students' achievements on exams, self-evaluation.
Other (as the proposer wishes to add)	